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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
09/765,166	01/18/2001	Ronald A. Fial	2000-0276	7479
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Samuel H. Dworetsky AT&T CORP. P.O. Box 4110 Middletown, NJ 07748-4110		EXAMINER LEJA, RONALD W		
		ART UNIT 2836 PAPER NUMBER		

DATE MAILED: 11/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

## Application No.

09/765,166

## Applicant(s)

FIAL ET AL.

## Examiner

Ronald W Leja

## Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 11 June 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-31 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 19-22 and 25 is/are allowed.
- 6) ☒ Claim(s) 1-11, 13-18, 23, 24 and 26-31 is/are rejected.
- 7) ☒ Claim(s) 12 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 January 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 1/18/01. 6) ☐ Other: \_\_\_\_\_

1. Claims 12, 19 and 23 are objected to because of the following informalities: In Claims 19 and 23, (AAC@) should probably be (AAC) and in Claim 23, (ADC@) should probably be (ADC). In Claims 12 and 19, under item (d), it is believed that the cathode of the clamping diode is connected to the gate of each of said first and second FET transistors and the anode is connected to the source of each of the first and second FET transistors. See Figures. Appropriate correction is required.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, 6-9, 11, 23, 26, 27 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Damiano et al. (4,626,954).

Damiano et al. disclose an AC power controller, which can detect a resistive load. See Figures 1, 2a & 2b. The Figures clearly illustrate multiple signal paths being connected between the various components of the processor. Since all paths and components are connected together, it is reasonable to consider that the signal and AC paths are all connected to the device input and to the device output. (SH) is the sensing resistor located between the two FETs (SW1) & (SW2). For Claim 2, there is a transistor (FET5) coupled to the gates of (SW1) & (SW2). The design includes a power supply

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circuit comprising a voltage rectifier (D1), a voltage regulator (ZD1,ZD2) and a filter (C1). See (ID1) and (ID2) for the parasitic diodes of Claim 8. See Figure 2a, the AVC circuitry for an amplifier circuit of Claim 9 and the ZVD circuitry for the zero crossing event detecting of Claim 11.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 10, 24, 28, 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Damiano et al..

Claim 10 requires that the detected current is unbalanced; Claim 24 requires that a resistor be connected to the FETs and to the switch

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and Claim 28 essentially adds A-to-D conversion. It is the opinion of the Examiner, that even though the reference is silent wrt unbalanced current, when a resistive load is detected, i.e. a person touching the line between the switches and load, that the detected overload current will be unbalanced, and as such, unbalanced load current detection is obvious in view of the teachings of the reference. Figure 2a illustrates the use of resistors (R39,R40) being connected between the controlling switches (FET5,FET6), respectively and sources of DC voltages. The resistors are for current limiting, and as such, placement of (R40) between (FET6) and the gates of the FETs (SW1,SW2), would have been an obvious modification, as a matter of engineering design choice, since such movement of the resistor would perform equally well. The use of A-to-D conversion is well known in the art and would have been obvious to apply if the processor components of Damiano et al. were replaced with a microprocessor, thereby gaining in space conservation. A plus for any engineering product design. As far as the detecting of positive and negative over-voltages of Claims 30 & 31, overvoltage detection is well known in the protection art, and as such, it would have been obvious to one having ordinary skill in the art to apply such protection to an AC power system as a means to offer a more fully protected load and power switches, resulting in a higher degree of reliability.

6. Claims 5 and 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Damiano et al. in view of Berry et al. (3,982,173).

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Claim 5 adds that the rectifier includes two diodes and 13 adds that the output of the rectifier passes through the regulator before being applied to the filter. Damiano et al. disclose one rectifier diode and filtering before use of a regulator. Berry et al. teach (see Fig. 4) production of DC voltage from AC voltages wherein more than one diode is utilized for the rectifier (18') and that regulation is accomplished before filtering (58'). Application of such teachings would have been obvious as a means to ensure delivery of the required amount of current and while simultaneously maintaining a substantially constant output voltage. (See Col. 7, lines 1-7).

7. Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claims 19-22 and 25 are allowed.

9. The following is a Statement of Reasons for the Indication of Allowable Subject Matter: The prior art of record does not disclose nor suggest the claimed combinations found within Claims 12, 19 and 25.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ronald W Leja whose telephone number is (703) 308-2008. The examiner can normally be reached on Monday thru Friday.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (703) 308-3119. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

  
Ronald W Leja

Primary Examiner  
Art Unit 2836

rwl  
November 2, 2003

